2023 11th International Conference on Internet of Everything, Microwave Engineering, Communication and Networks (IEMECON) | 978-1-6654-7512-9/23/$31.00 ©2023 IEEE | DOI: 10.1109/IEMECON56962.2023.10092307

FPGA-Supported HDL Approach to Implement Reversible Logic Gate-Based ALU

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Abstract— ***This manuscript banks on the design of reversible gates and implementation of an Arithmetic Logic Unit – 16 bit (ALU) utilizing Verilog with Xilinx ISE 14.7, Spartan 6 FPGA kit. The same functionality is compared with a basic logic gate-based ALU. Reversible gates can producea distinct output vector from each input vector, and the opposite is also possible. Circuits with irreversible gates suffer from data erosion. Power loss results from a circuit's loss of data. In conclusion, gates with reversible logic are preferable over irreversible counterparts. A library of reversible gates, comprising of AND, OR, NAND, NOR, and XOR, using Verification Logic Hardware Description Language (HDL) is developed, which in turn contributes to the designing of arithmetic and combinational logic like full adder, decoder (2:4), decoder (3:8), multiplier, full subtractor, and comparator.***

Keywords—Verilog, Xilinx ISE, Toffoli Gates, FPGA Spartan 6.

I. INTRODUCTION

Modern computers squander a lot of power and storage space. Every instant, they discard millions of bits. These are built on irreversible logic units, which have been acknowledged for a significant period to be essentially wasteful energy-wise. The optimum solutions are hence reversible gates. Losses are kept to a minimum in circuits with reversible gates. The number of inputs and outputs in these circuits will be identical, and the vectors of inputs and outputs will be mapped one to one [1]. Examples of such gates are Fredkin, Toffoli, Interaction, and Switch.

A full adder is a digital arithmetic logic circuitry that accumulates n input bits along with a carry. Adder circuits are included in a wide range of processing devices, not simply ALU-related tasks, to calculate various increment or decrement calculations, addresses, and others. A device designated as a multiplexer has numerous inputs but just one output. After selecting one from the many analog and digital inputs, the detected inputs are then forwarded a single line [2]. A combinational logic circuit such as a binary decoder translates binary data from n number of inputs to a maximum of 2^n distinct outputs. In analogue decoders, the decoders are utilized in the analog-to-digital transformation process.

A full subtractor deducts n input bits while taking borrow into account. They are employed in digital electronics applications and calculations involving mathematical operations. A combinational circuit identified as "Comparator-Comparator" analyzes n input bits and produces three different outputs: smaller, more robust, and comparable to devices used in analog-based applications.

Although there might be uses for reversible computing in transaction processing and computer security, its primary long-term advantages will be realized in fields that desire high levels of energy effectiveness and significant performance with speed [3,4].

II. GATES WITH REVERSIBLE LOGIC OVER IRREVERSIBLE COUNTERPARTS

Researchers have recently looked into several reversible logic gates and all solutions. Process enhancements ultimately come to an end. Energy use will grow unaffordable. Problems with heat dispersion will worsen. A traditional computer uses a lot of electricity—electron processes in bulk. To perform a single logical process, several electrons were employed.

III. METHODOLOGICAL ANALYSIS

With FPGA Spartan 6 and XILINX ISE version 14.7, applications like complete adders and multiplexers are implemented. A piece of software developed by Xilinx for the synthesis and evaluation of HDL designs is called Xilinx ISE. The developer can use this tool to synthesize their designs, run time analyses, look at RTL diagrams, design responses to various stimuli, and work with the coder to establish the intended device. A hardware kit called Spartan 6 FGPA is utilized to put developer designs into practice. Utilizing VHDL and Verilog HDL, this kit is simple to use and can implement any complicated circuit [5].

Steps to follow in descending order:-

1) A folder is created in a particular drive, and then the same is located as we enter the XILINX suite.
2) The new project will have a Spartan 6 with XC6SLX4 and TQG144 as the device and package and the language selected as Verilog.
3) The appropriate HDL code is written and simulated as behavioral in the new module.
4) Synthesis is done by forcing the inputs, henceforth generating the program file.
5) The latter is configured, and the outputs are checked on the FPGA kit.

IV. HDL SIMULATED REVERSIBLE LOGIC GATES

The reversible Toffoli logic generates the library, which includes the Toffoli-based basic and universal gates.

According to elementary physics, each time a bit of data is obliterated, energy should therefore be lost in a proportion equal to kT ln 2 per bit purged, where k is the Boltzmann constant and T is the absolute temperature (in Kelvin). Because data erasure causes inevitable energy losses, although all other energy loss techniques were removed from any NAND-based circuit, the circuit would still lose energy when it was in operation. The energy expenditures caused by logical irreversibility in NAND-based logic circuits nowadays are eclipsed by other loss sources. The energy losses caused only by information wiping, resulting from employing irreversible logic gates, will eventually become the main contributor as these other loss causes are subdued. The difficulties of extracting this undesirable surplus heat from deep inside the irreversible circuitry will now prevent further downsizing of technology nodes if nothing is considered today.

Execution of Libraries for the different logics: Toffoli-based Basic (AND, OR), Universal Gates (NAND, NOR), and CNOT. The inputs are considered as A, B, and C for every case [6-8]. Considering the library for all the gates implemented by the Toffoli gates, also known as the Controlled Controlled NOT gate (CCNOT), which is both reversible and universal, as shown in Fig. 1(a). Reversibility leads to no data loss, which finally contributes to no loss of power. Here the TRUE values of A and B will lead to the flipping of C. Since A and B are still present and can be used to reassemble C, this gate is reversible. Furthermore, since we can convert this gate into a NAND gate, it is universal, as depicted in Fig. 1(b). In building every plausible circuit, one NAND is sufficient. But even with just one Toffoli gate, we can effectively construct NOT, AND, and XOR. The NOT specific case of NAND should be acknowledged.Fig.1(c),(d),(e) shows the Toffoli NOT, Toffoli AND, and Toffoli XOR, and Fig. 2(a), (b), (c), (d), (e), and (f) displays the waveform simulated in Xilinx ISE 14.7 and further synthesized in FPGA Spartan 6.

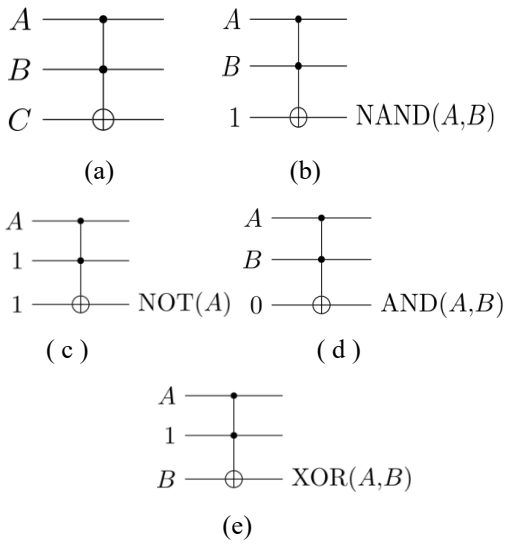

Fig. 1.(a) Toffoli Gate; (b) Toffoli NAND; (c) Toffoli NOT; (d) Toffoli AND; (e) Toffoli XOR.

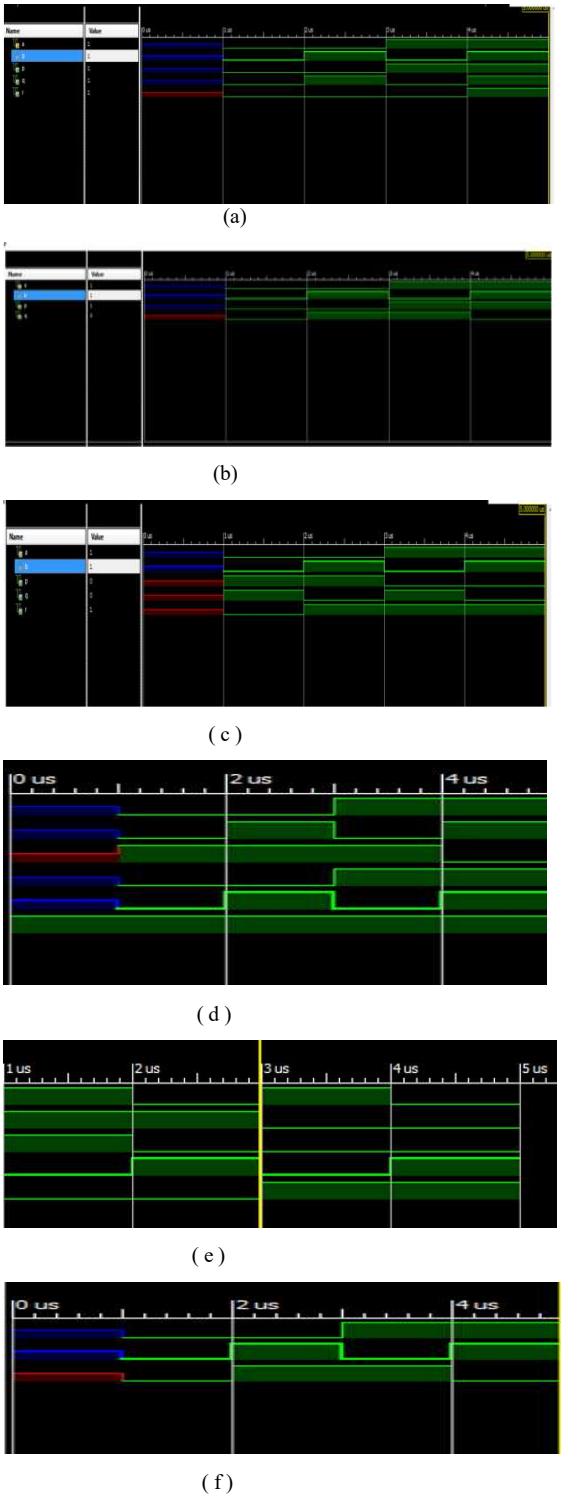

Fig.2. Simulated Waveforms for (a) Toffoli AND; (b) CNOT; (c) Toffoli OR; (d) Toffoli NAND; (e) Toffoli NOR; (f) Toffoli XOR

Contributions in the Digital circuits, both arithmetic and combinational, have been illustrated in the simulated XILINX ISE 14.7 waveforms in Fig. 3.

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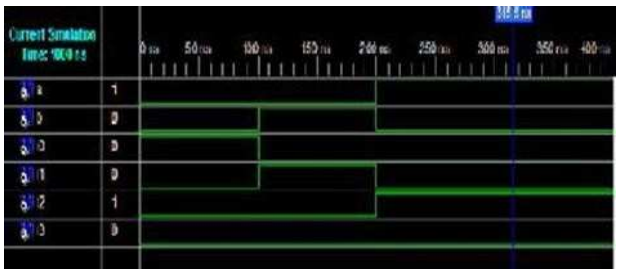
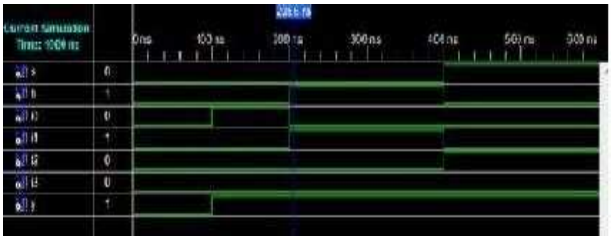


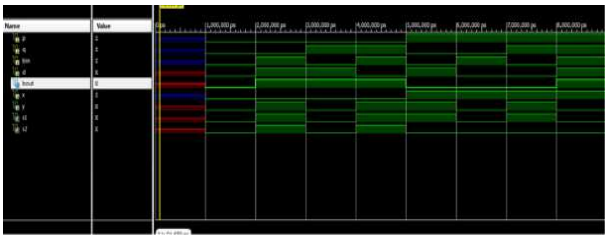
(a)

(b)

(c)



(d)



(e)

Fig.3. Simulated Waveforms for (a) 2:4 Decoder; (b) 3:8 Decoder; (c) Full Adder; (d) Multiplexer; (e) Full Subtractor

Scientists have recently looked into various reversible nature logic gates and associated equivalents. Our solution has the benefits of being deployed at the gate level and having basic, straightforward logic that is simple to build. The circuits are created with the fewest possible gates. While we implemented using 2-3 (least) no of gates, such as 1 TR gate, 1 Feynman, and 1 BJN gate, the current comparator designs utilize more no. of gates, including 8 to 9 TR gates in comparison. As indicated in the reference, full subtractors and adders are created using nine gates, making the design challenging for simulation and coding. Three gates have been simplified and integrated into our unique ways. Therefore, the study of graphs and GNR used as connections could be a further study of this research.

V. REVESIBLE GATE BASED 16-BIT ALU

A highly engineered arithmetic circuitry with the fewest clock cycles feasible that can execute basic arithmetic tasks as well as the square, square root, and inverse. In this research, the ALU was designed with superior productivity and trial ability in mind. For the development of an elevated arithmetic unit, layouts with a significant level of concurrency were investigated. Operational entities were created with an 8-bit capability for convenience. Increased operand capacity might necessitate hardware duplication in parallel with current circuitry owing to architectural symmetry. The ALU features an isolated gear that can compute square, square root, and inverted in addition to executing fundamental integer arithmetic tasks. Using logic cells from the integrated cell catalog, an 8-bit logic unit was constructed, and it was discovered that it operated at a peak frequency of almost 1GHz. A unified ADD or SUB unit was used to build for addition and subtraction operations. A number's 2's complement is created by erasing the operand and then incrementing by 1. If the Control (CTRL) signal is "Strong," the XOR gate flips the second input. C_{in} receives the control command to execute the necessary adjustment for the two's complement computation.

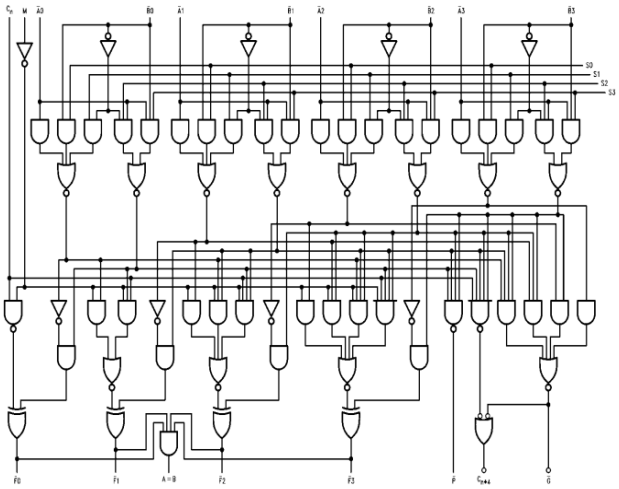


Fig.4. Architecture for Arithmetic Logical Unit, based on Irreversible gates

Fig.4. shows the logic diagram for a regular irreversible gate-based ALU capable of performing about 16 instructions, such as the comparison as well as the basic gate-related operations, i.e.:- AND, OR, NOT, and the universal gate based such as the NAND, NOR. We utilize 3*3 Toffoli gates in a 3×3 matrix. NOT gates cascade the reversible and function generator and controlled unit to create the bidirectional Arithmetic Logical Unit with the lowest possible expense, depicted in Fig.5.. Additionally, cascading can be employed to construct the ALU units that can reverse any number of bits, as shown in Fig.5. The ALU, in reversible mode undertake activities in the range of A_7 to A_0 and B_7 to B_0 for A and B respectively.

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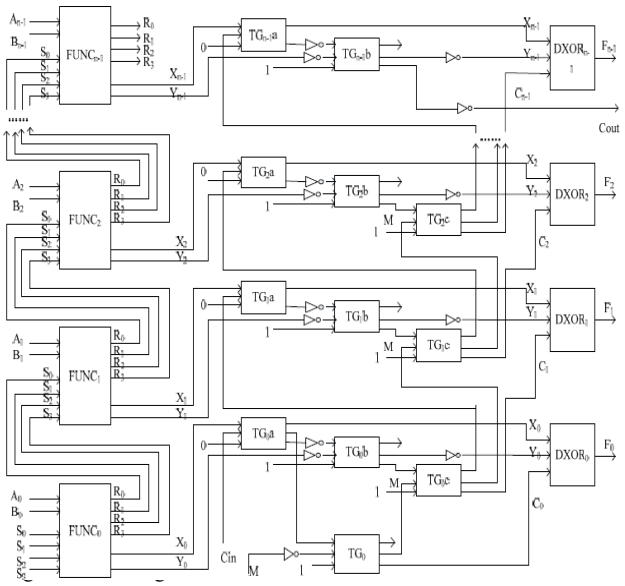

The consequence of the first and the second inputs of the control unit of reversible type, $DXOR_{(0\text{-}7)}$ are equal to the value of the function generator, $FUNC_{(0\ \text{-}7)}$ outcome X_i and Y_i. The value of the third input control, C_i of reversible controlled unit $DXOR_{(0\text{-}7)}$ has some connection with the control signal, namely M.

A. ALU using irreversible gates

Considering 0 and 1 as inputs for M and C_{in}, the value is obtained in the output as F and C_{out}, and figure 6 shows the output waveform for basic logic gate-based irreversible ALU.

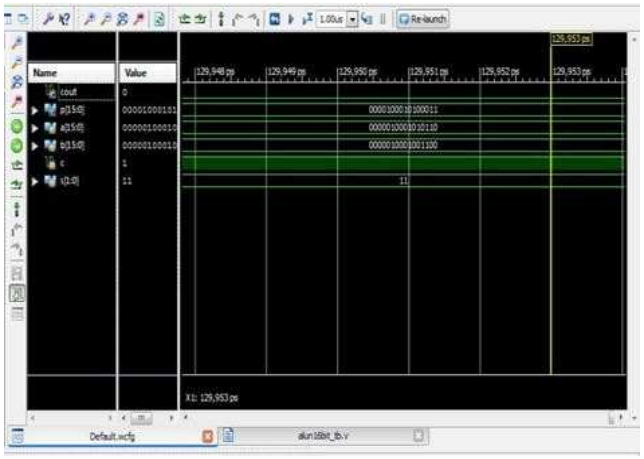

Fig.6. Waveform for ALU based on the irreversible gate

B. ALU using irreversible gates

The output waveform layout of a 16-bit irreversible adder and subtractor is illustrated in Fig. 7. The inputs as A and B for the module and M as a control indicator in the 16-bit data. The addition process is carried out whenever the control input is "Low" and the subtraction operation when the same is "High." "C_{in}" and "C_{out}" denote the carry-in and borrow-out, respectively, for the proposed circuit

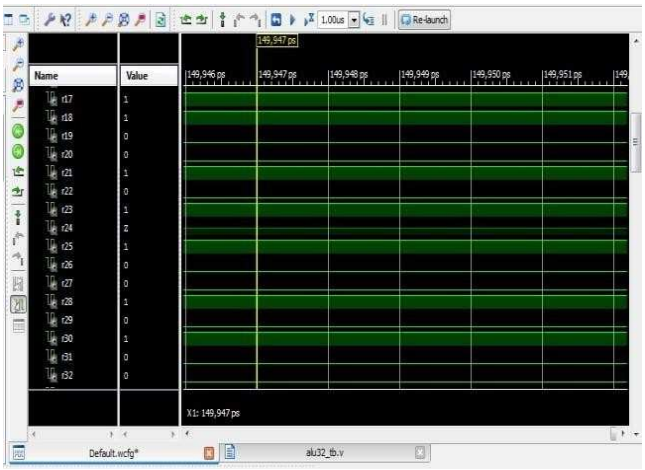

Fig.7. Waveform for ALU based on the reversible gate.

Table 1: Power and Delay contrast

Method for ALU Design	**Power (ns)**	**Delay (mW)**
Using Irreversible Gates	2.301	0.320
Using Reversible Gates	1.801	0.247

VI. RESULT AND DISCUSSION

Among the low-power techniques, Toffoli logic gates are utilized to lower the power consumption compared to logic gates of irreversible nature. The implementation of an ALU relying on reversible circuitry minimizes the power utilization during computations to around 7.3%, as indicated in Table 1. At the same time, an ALU developed employing non-reversible logic gates consumes additional power of about 0.320 mW.

VII. CONCLUSION

In this research, we suggest adopting reversible logic gates rather than conventional gates to design and synthesize a 16-bit reversible ALU. Reversibility significantly lowers data bit usage and degradation, resulting in optimal power consumption. With the help of Xilinx ISE 14.7, diverse modules' efficiency is examined. Reversible logic-based circuit designs displayed decreased power and latency. The topic of study has been logical reversibility, or the ability of inputs and outputs to be separately retrieved from one another.

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