REVERSIBLE ADDER DESIGN FOR RIPPLE CARRY AND CARRY LOOK AHEAD (4, 8, 16, 32-bit)

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***Abstract*—Reversible logic has represented itself as a prominent technology which plays an important role in Quantum Computing. Theoretically Quantum Computers operates at high speed and consumes less power. Furthermore, Reversible logic can break the conventional speed of power trade-off. To prove this we are implementing Ripple Carry Adder and Carry Look Ahead Adder using reversible logic gates. The paper presents efficient adder circuits using Peres gate, New fault Tolerant gate and Double Feyman gate. The complexity, simulated outputs and the speed parameters for the adder circuit have been indicated using the Quartus II 9.1 edition and Modelsim tool.Moreover, the quantum algorithms can potentially solve NP-complete problems. Furthermore, doing high performance functions beyond the limit of deterministic computer systems is possible by only reversible logic. Quantum operations are unitary in nature which is reversible and hence the arithmetic operations like adders can be implemented using the reversible logic.**

Likewise, optimized block size, minimum ancillary bits, and one to one mappings of inputs and outputs are obtained in the reversible adder circuit, giving fan out as 1. Hence, the Ripple Carry Adder and Carry look Ahead Adder is providing complexity reduction and high speed, proving to be an efficient and important part in the development of arithmetic blocks of Quantum Computers.

Keywords—Reversible logic gate, NP-problems, Quantum Computers, time complexity, unitary operations

I. INTRODUCTION

The advancement in the very large scale fabrication process and integration technologies has resulted in better logic circuits and faster logic switching. The faster logic switching results in higher energy dissipation as proved by 'Landauer'[5]. He proved that a KTln2 joule of heat energy was generated while logically computing bitwise loss of information. Where k is known as the Boltzmann's constant and has a value of 1.38 x 10^{-23}J/K, and T is the absolute temperature of the environment. So we can reduce the energy dissipation by improving the method of erasing the logic bit. It is proved by 'Benett'[3] that if the logic circuits consist of only reversible gates, the power dissipation can be zero. Furthermore, no information is erased by reversible logic and in principle they can dissipate arbitrary little heat. This is why the use of reversible operations is likely to become more attractive.

Reversible circuits are also called as lossless circuits as there is neither energy loss nor information loss. Faster Logic implementation is possible by the use of quantum computation. Quantum computation requires use of four bits to represent logic bit instead of logic 0 and 1. These quantum bits are called qubits. This is a futuristic approach to develop quantum computers. The Quantum computation requires one to one mapping between inputs and outputs. The reversible logic circuits have three major principles-

(i) There must be one to one mapping between inputs and outputs i.e. there must be a unique output vector for unique input vector,

$$I_x = [I_1, \quad I_2, \ I_3, \ldots\ldots \ I_n]$$

$$O_y = [O_1, \quad O_2, \ O_3, \ldots\ldots \ O_n]$$

(ii) Each output bit must drive a single input line for further stage, i.e., the fanout must be 1.

(iii) The garbage bits should be minimum.

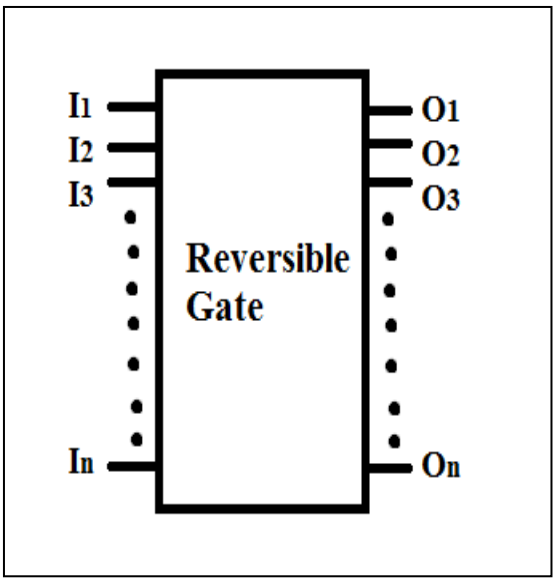

*Fig.1.*Basic Reversible Gate

Reversible Logic has also found applications in several disciplines such as DNA technology, quantum computing, nanotechnology, and optical computing.One or more operations can be implemented using single reversible logic gate.

II. SOME DEFINITIONS USED IN THE PAPER

Definition 1

Gate: A gate is said to be reversible gate if it consist of unique vector outputs for unique vector inputs and vice versa.

Definition 2

Garbage Output: A Garbage output is the output that is not utilised to drive an input of further gate, but we need them so that we can retrieve the inputs through the reversible gates from its outputs.

Definition 3

Ancilla Bits: This is the constant high or low inputs provided at few pins of reversible gates.

Definition 4

Acyclic: Feedback circuitry is not possible in reversible logic

Definition 5

Quantum cost: The number of 1X1 and 2X2 reversible gates or quantum logic used and design.

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III. PROMINENT REVERSIBLE GATES

Some of the prominent reversible gates employed to design the adders are mentioned in this section

A. FEYMAN GATE

The Fundamental 2*2 reversible logic gate is Feyman gate

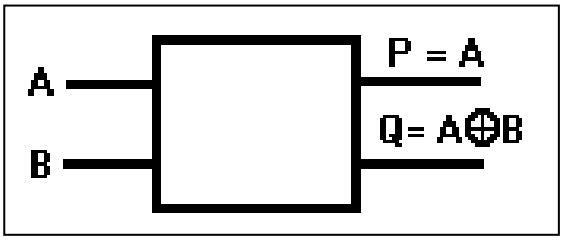

Fig. 2Feyman Gate

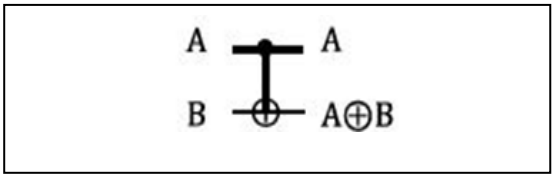

*Fig.*3.Quantum representation of Feyman gate

B. DOUBLE FEYMAN GATE

The 3*3 Feynman double gate with quantum cost of 2 is shown in figure4.

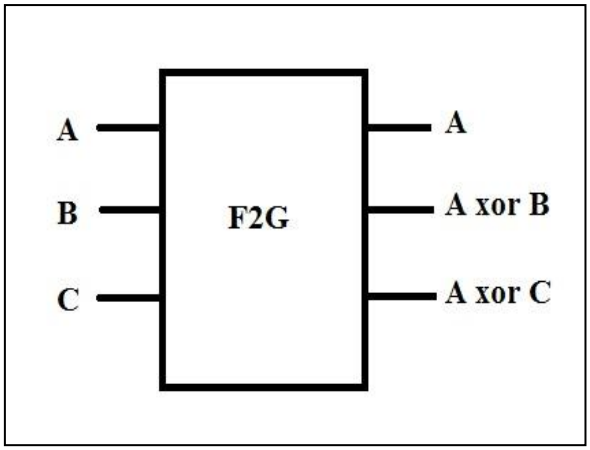

Fig. 4.Double Feyman Gate block diagram

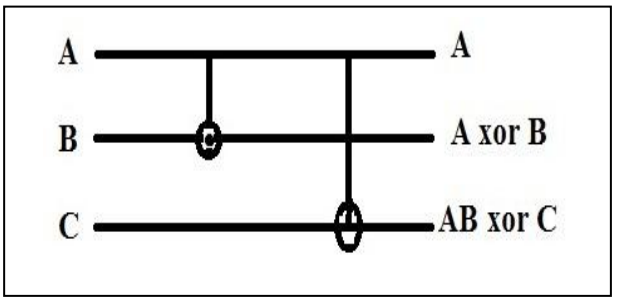

Fig. 5 Quantum representation of F2G gate

C. PERES GATE

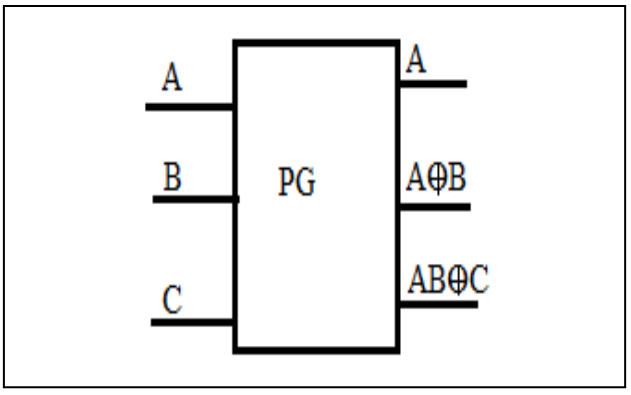

Fig.6 Peres gate block diagram

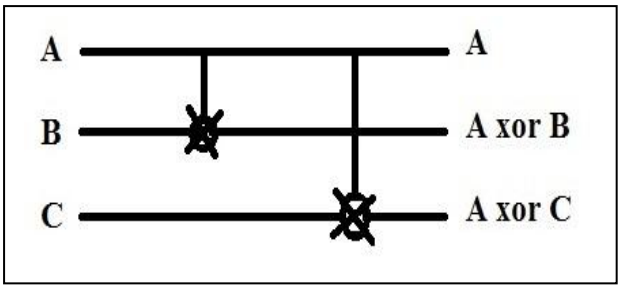

*Fig.*7 Quantum representation of Peres gate

D. NEW FAULT TOLERANT GATE

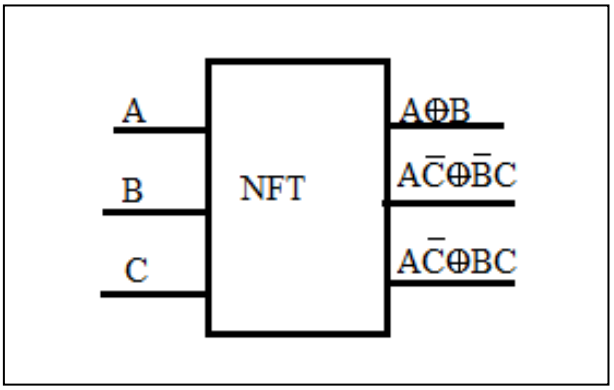

*Fig.*8New Fault Tolerantgate block diagram

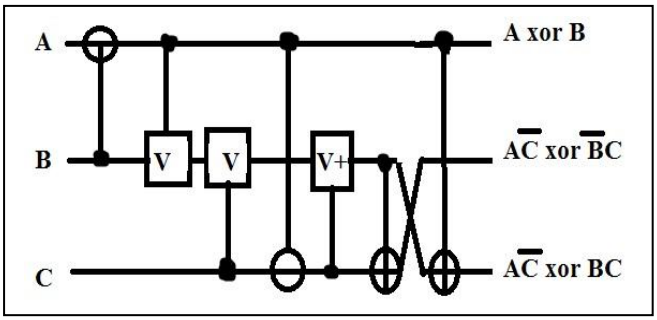

*Fig.*9 Quantum representation of NFT gate

IV. PROPOSED CIRCUIT DESIGN

A. *RIPPLE CARRY ADDER*

Full adder is a basic unit for both adder RCA and CLA. Modified realization of reversible full adder circuit using two 3*3 Peres gate is shown in figure10. This circuit minimizes the count of gate, garbage outputs, and constant input. It has been proved that reversible full adder circuit can be realized with at least two garbage outputs and one constant input. When creating the full adder, the third input is considered as zero for first Peres gate. Thus its outputs are:$P = G1$; $Q = A \wedge B$; $R = A.B$

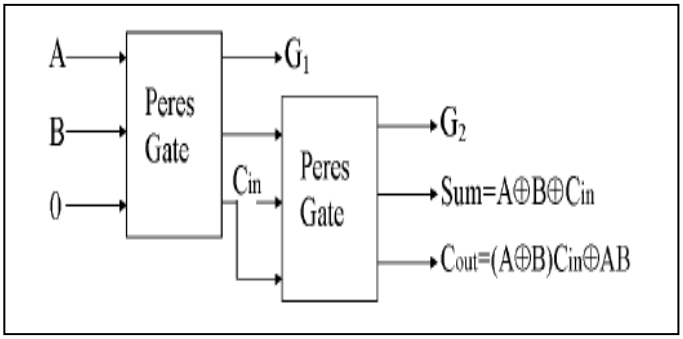

*Fig.*10.Bit full adder using PG gate

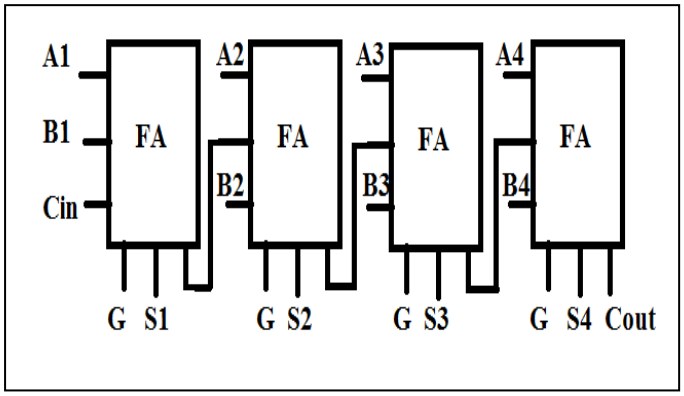

*Fig.*11. Four Bit full adder

The outputs of single bit Ripple carry adder are as represented as follows

$$Sum = A \oplus B \oplus C$$

$$Carry = (A \oplus B).Cin \oplus AB$$

Table ITwo-Bit full adder Truth table using Peres Gate

A	B	C	G1	G2	SUM	COUT
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	1	0
0	1	1	0	1	0	1
1	0	0	1	1	1	0
1	0	1	1	1	0	1
1	1	0	1	0	0	1
1	1	1	1	0	1	1

A Ripple Carry adder requires n full adder circuits. The RCA propagates the carry input through each full adder logic block. The carry out of the i_{th}full adder is connected to the $(i+1)_{th}$ full adder. Thus the next block has to wait for the previous logic block to provide the carry input for that particular stage. It provides the sum and carry after n-stages for n-bit addition. The output Q and R of 1st PG are applied to input A and C of 2nd PG resp. The sum and carry hence generated at final stage are same as that of generic CMOS full adder. The paper proposes architecture for 4 bit, 8bit, 16 bit and 32 bit ripple carry adder, and calculation of delays and complexity in these circuit.

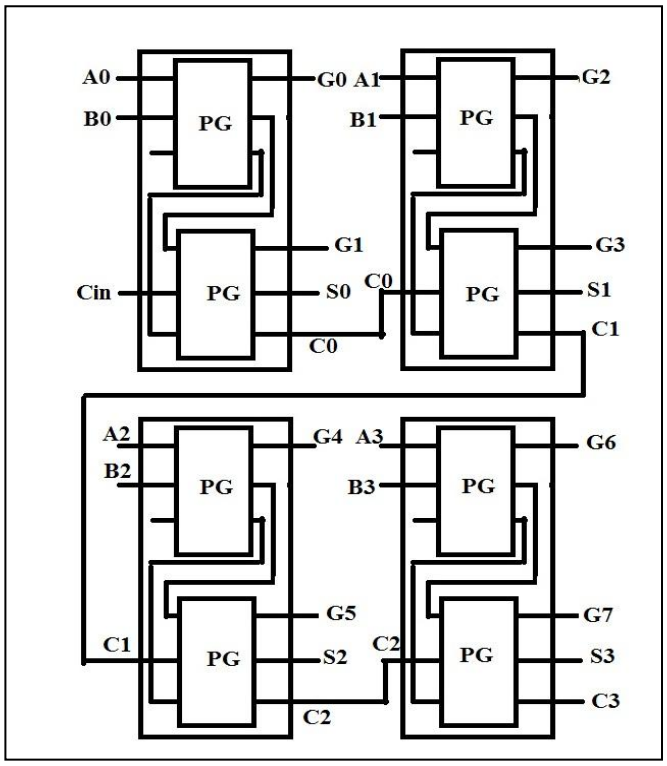

*Fig.12*Block diagram of proposed 4-bit ripple carry adder

B. CARRY LOOK AHEAD ADDER

Parity checking is the basic technique in finding error in digital communication. Here we are using new fault tolerant gate and double Feyman gate for implementation of carry look ahead adder. The purpose of selection of NFT is that it preserves the parity bit if there is no fault detected at signal level, hence no intermediate checking will be required. This paper presents a 32-bit reversible carry look ahead adder that is efficient in terms of delay and hardware complexity.

It is not possible that all reversible logic gates will be preserving parity bit. But both gate used here in CLA are parity preserving gate hence the whole adder preserves the parity. The prime purpose behind addition using carry look-ahead is an attempt to generate all incoming carries in parallel and avoid waiting until the correct carry propagates from the stage (FA) of the adder where it has been generated.

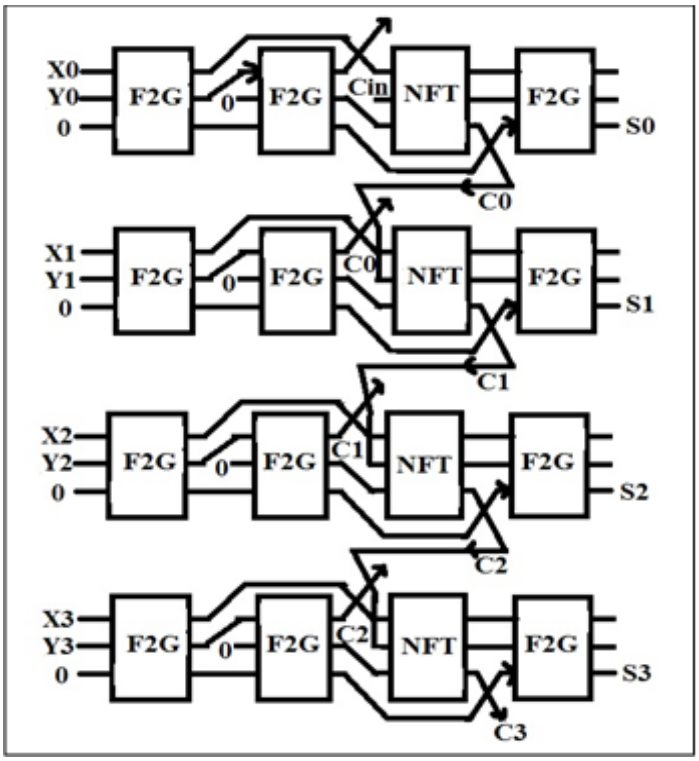

Fig.13 Block diagram of proposed 4-bit carry look ahead adder

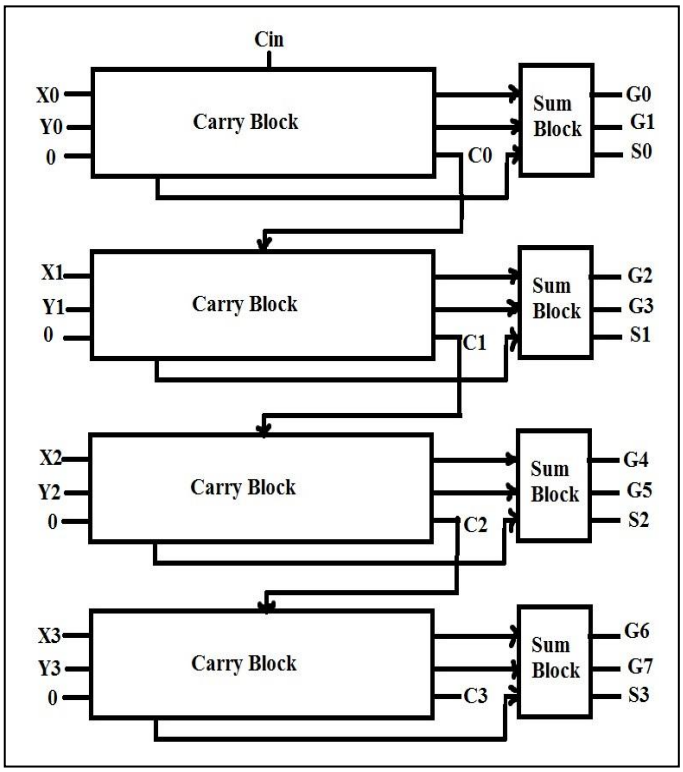

Fig 14. Generalised Block diagram of proposed 4-bit carry look ahead adder

V. SIMULATION RESULTS

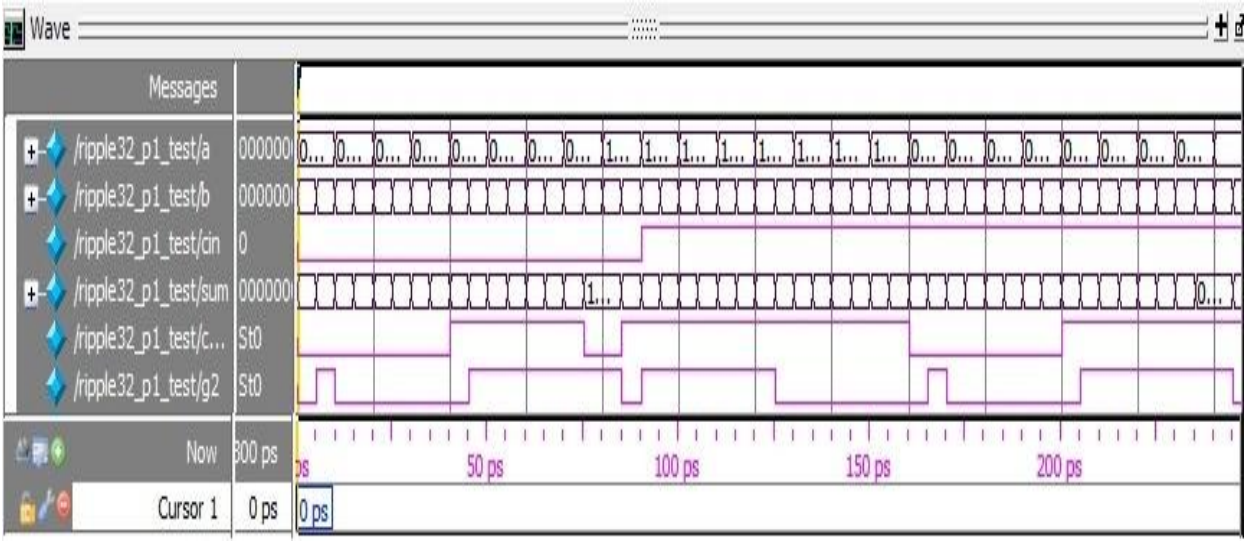

Fig 15.simulated output for 32 bit ripple carry adder

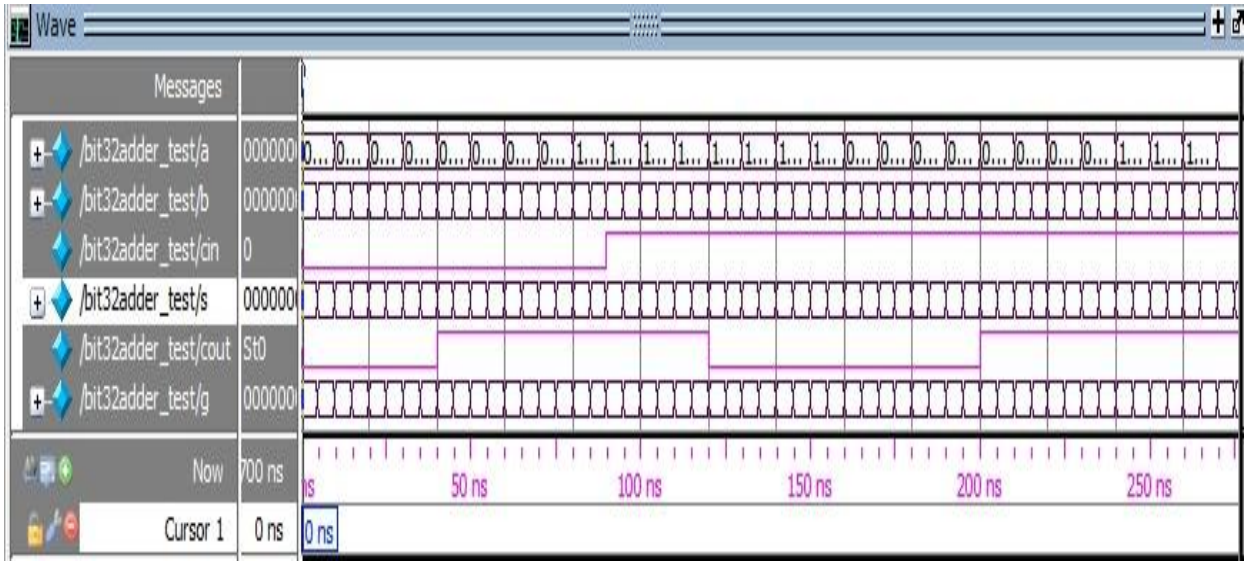

Fig 16. Simulated output for 32 bit carry look ahead adder

TABLE II Delay and Complexity outputs

S.No.	N-Bit	Ripple Carry Adder		Carry Look Ahead Adder	
		Delay	Complexity	Delay	Complexity
1.	4-bit	13.153 ns	12α+8β	10.048 ns	28α+16β+4δ
2.	8-bit	17.474 ns	24α+16β	14.133 ns	56α+32β+8δ
3.	16-bit	24.022 ns	48α+32β	21.303 ns	112α+64β+16δ
4.	32-bit	35.414 ns	96α+64β	33.962 ns	224α+128β+32δ

VI. CONCLUSION

This paper has emphasis on the efficient approach for designing reversible ripple carry adder and carry look-ahead adder.The designs imply that their outputs contain as much information as their inputs and thus, according to Landauer's[5] principle, that they (at least in principle) can operate with arbitrarily low dissipation. These adderscan be used further as an indispensable part of future development on Quantum computers. The proposed design is optimized in terms of delay and hardware complexity. Firstly, the gate used here, in carry look ahead adder are parity preserving gate, hence the whole adder preserves the parity. Therefore, no intermediate checking will be required if there is no fault detected. Secondly, the circuitry for reversible ripple carry adder generates less complexities and delays, hence proving to be a valuable asset in being an integral part of the Quantum computer blocks. By integrating the proposed design parallel processing in adding the input has been achieved.

VII. FUTURE SCOPE

Now days the prime focus is on achieving less delay and reduce in complexity of circuit. This helps in kick starting the fast processing environment. Not only saving the time consumed in calculating the output will be less, but also the probability of solving NP-complete problems will be more. In the case of convention circuits, due to their non-reversible behaviour there is information loss. Furthermore, as data has to be reloaded often between input and output vectors of communication channels, there is an ample amount of energy dissipation in the circuit. This paper can be further extended for digital design development using reversible logic circuits which are useful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. Furthermore the delay and complexity of reversible logic gates, compared to those of conventional is less which is desired for the fast and gradually compacting chips. Thus, the reversible logic will become increasingly "hot" in the near future.

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