

# Reversible Full Adder/Subtractor

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**Abstract**—This paper proposes two novel designs of Adder/Subtractor using reversible logic gates. The first design is an implementation of two's complement Adder/Subtractor suitable for signed/unsigned numbers. The other design proposes a novel reversible gate that can work singly as a reversible Full Adder/Subtractor unit. The proposed Full Adder/Subtractor is then applied to design a reversible 4-bit ripple Adder/Subtractor.

## I. INTRODUCTION

Reversible computing is a promising area of a study. According to Landauer's research, the amount of energy dissipated per irreversible bit operation in thermodynamic entropy is at least  $kT \ln 2$  joules, where  $k$  is Boltzmann's constant, and  $T$  is the temperature of the environment [1][4]. Bennet [8] argued that energy dissipation would be zero only if the network consists of reversible gates, so reversible computing will become very important on the future days in circuit design.

Various technologies for reversible logic are recently intensively studied. These technologies include: Standard CMOS, Optical technologies, Quantum logic technologies, DNA technology and Mechanical technology (nanotechnology) [2]. The most prominent application of reversible logic lies in quantum computers [5]. Quantum arithmetic must be built from reversible logical components.

In this paper, we proposed two novel designs of Adder/Subtractor using reversible logic gates. One of the designs is based on FG gate and HNG gate. The other design is based on a novel reversible gate which can work singly as a reversible Full Adder/Subtractor.

The rest of the paper is organized as follows: Section II provides the necessary background on reversible logic. Section III provides the popular reversible logic gates found in the literature. Related work can be found in Section IV. Section V discusses the proposed circuits. Section VI concludes our work.

## II. REVERSIBLE GATES

The circuit (gate) which is bijective and doesn't lose any information is called reversible gate [3][4].

Mozammel [2], Hafiz et. al.[3] and Majid and Keivan[4] defined circumstances for any gate to become reversible gate as follows:

- Number of input and output lines must be the same.
- Feedback (loop) is not allowed in reversible logic.
- Fan-out is not allowed in reversible logic; Fan-out is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.
- One of the major constraints in reversible logic is to minimize the number of reversible gates used.
- Minimizing the garbage outputs produced; Garbage output refers to the output that is not used for further computations. Garbage is the number of outputs added to make an  $n$ -input  $k$ -output Boolean function  $((n,k)$  function) reversible [3].
- Using minimum number of input constants.

The following is an example of a reversible gate. Consider the XOR gate; Table I.a represents its truth table. From this truth table, we can't know the input which gives us 0 output, so it is not one to one mapping. It is not a valid truth table of a reversible gate.

TABLE I. TRUTH TABLE OF REGULAR XOR AND REVERSIBLE XOR GATE

Inputs			Outputs	
A	B		$A \oplus B$	
0	0		0	
0	1		1	
1	0		1	
1	1		0	

(a)

Inputs			Outputs	
A	B	X	$A \oplus B$	
0	0	0	0	
0	1	0	1	
1	0	1	1	
1	1	1	0	

(b)

Table I.b represents it by a reversible logic gate. From each output, one can know the corresponding input. X is a garbage output. It is added to make one to one and onto mapping.

### III. POPULAR REVERSIBLE LOGIC GATES

Many reversible logic gates are found in the literature and some of the popular reversible logic gates are listed below:

- 1 \* 1 NOT gate: It is the simplest among all the reversible logic gates where the gate has only one input (A) and one output (B) such that  $B = \overline{A}$  [3].
- New Gate[13] shown in Figure1

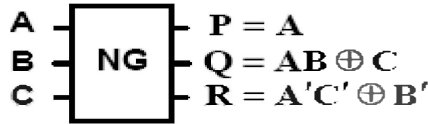


Figure 1. New Gate

- Feynman Gate[14][15] shown in Figure2

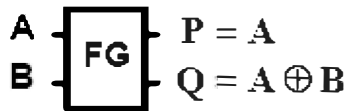


Figure 2. Feynman Gate

- Toffoli Gate[12][6] shown in Figure3

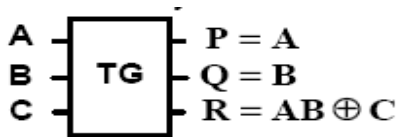


Figure 3. Toffoli Gate

- Peres Gate OR New Toffoli Gate Combining TG and FG[10] shown in Figure4

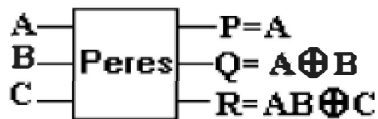


Figure 4. Peres Gate

- Fredkin Gate[12][7] shown in Figure5

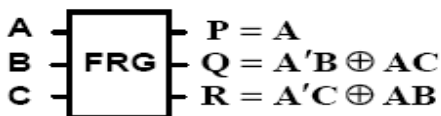


Figure 5. Fredkin Gate

- HNFG Gate[4] shown in Figure6

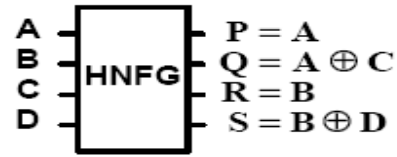


Figure 6. HNFG Gate

- HNG Gate[4] shown in Figure7

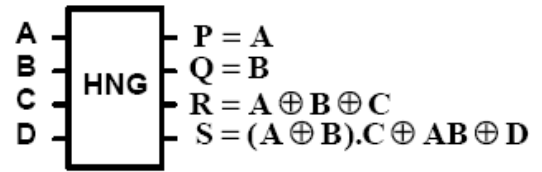


Figure 7. HNG Gate

- NFT Gate[9] shown in Figure8

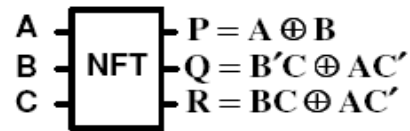


Figure 8. NFT Gate

- TSG Gate[11] shown in Figure9

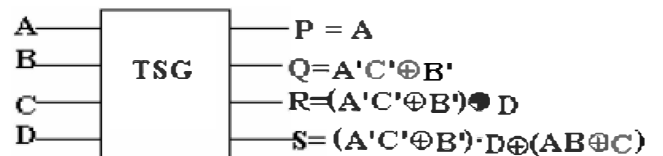


Figure 9. TSG Gate

### IV. RELATED WORK

To our knowledge, no design for reversible Full Adder/Subtractor found in the literature but there are many different designs for reversible Full Adder only [2], [3], [4], [11], [12].

Our first design (circuit 1) uses the HNG gate of Majid and Keivan[4] which can work singly as a reversible Full Adder unit as shown in Figure10.

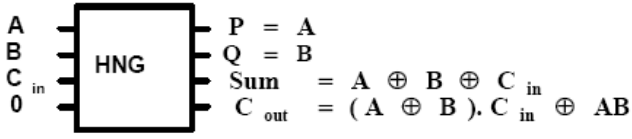
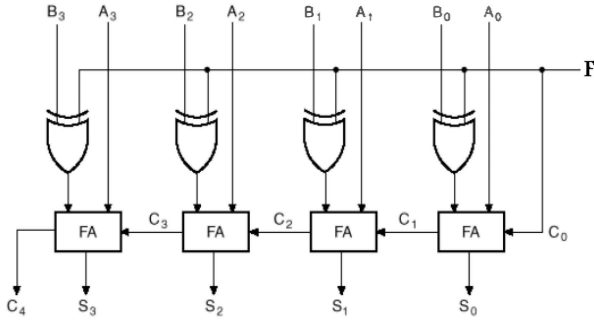


Figure 10. HNG gate as Reversible Full Adder



## V. PROPOSED CIRCUITS

### A. The First Design of Reversible Full Adder/Subtractor (Circuit 1)

This design implements the addition and subtraction of signed/unsigned numbers. Our design is based on the Adder/Subtractor circuit [16] shown in Figure11.

Figure 11. 4-bit Ripple Adder/Subtractor with combinational gates

The XOR gate is replaced by Feynman reversible gate (FG) with 2 inputs, flag (F) and B, and 2 outputs, G (garbage) and B or  $\bar{B}$  depending on the value of flag (F) input. If  $F = 0$ , B passes to the second output, otherwise,  $\bar{B}$  passes. The Full Adder in Figure11 is replaced by HNG gate. It has 4 inputs; one of them is the constant 0 and the other inputs are B or  $\bar{B}$ , the output of Feynman reversible gate (FG), A and carry (C<sub>in</sub>). Its 4 outputs are B, A which are 2 garbage, sum/diff (S/D) and carry (C); this can be shown in Figure12.

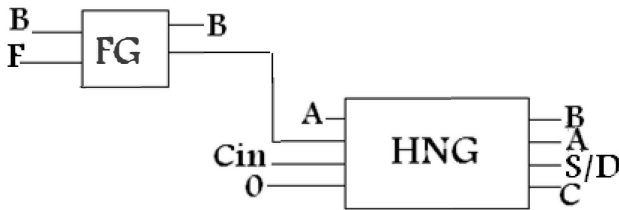


Figure 12. Reversible Full Adder/Subtractor (circuit 1)

The 4-bit reversible Ripple Adder/Subtractor shown in Figure13 (circuit1).

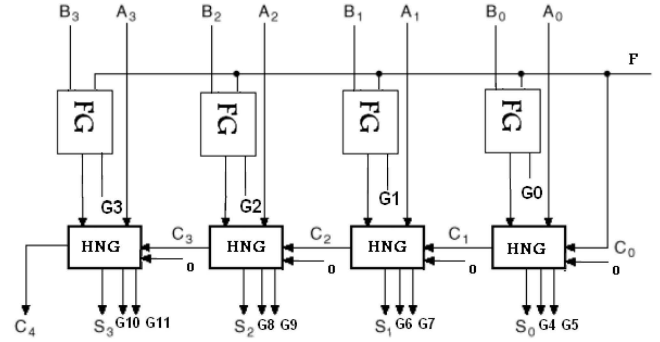


Figure 13. 4-bit reversible Ripple Adder/Subtractor (circuit 1)

### B. The Other Design of Reversible Full Adder/Subtractor (Circuit2)

A novel reversible gate is proposed to implement Full Adder/Subtractor. The truth table for Full Adder/Subtractor is shown in Table II, where A, B are the number to be added/subtracted and C is the carry/borrow from previous stage. The outputs are the sum S, the carry C, the difference D and the borrow B.

TABLE II. TRUTH TABLE OF REVERSIBLE FULL ADDER-SUBTRACTOR

Inputs			Outputs			
A	B	C	S	C	D	B
0	0	0	0	0	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	1	0	0	1	0	0
1	1	1	1	1	1	1

This table is modified to be bijective as follows. Another input (F) is used as a flag to determine whether to add or subtract. The first output is for sum (S)/difference (D) as they are always equal for the same input. The second output is for carry (C)/borrow (B). It represents the carry when  $F = 0$  and the borrow when  $F = 1$ . The other two outputs are garbage. They are chosen as A and  $F \oplus B$ . The modified truth table is shown in table III. It corresponds to the proposed ADD/SUB reversible gate shown in Figure14. It has 4 inputs; Flag (F) to determine whether the ADD/SUB gate will work as Adder or Subtractor, A and B are the numbers to be added or subtracted and C is the carry or borrow bit. It has 4 outputs, S/D for sum/difference, C/B for carry/borrow, A and  $F \oplus B$ .

TABLE III. TRUTH TABLE OF NOVEL REVERSIBLE ADD/SUB GATE

Inputs				Outputs			
F	A	B	C	S/D	C/B	A	$B \oplus F$
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	1	0	0	1
0	0	1	1	0	1	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1
1	0	0	1	1	1	0	1
1	0	1	0	1	1	0	0
1	0	1	1	0	1	0	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	1	1	1	0

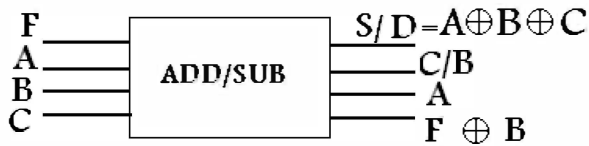


Figure 14. The novel reversible ADD/SUB gate (circuit 2)

When  $F = 0$  in ADD/SUB gate, it works as Reversible Full Adder as shown in Figure 15 and when  $F = 1$ , it works as Reversible Full Subtractor as shown in Figure 16.

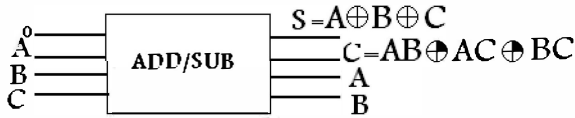


Figure 15. Reversible Full Adder with ADD/SUB gate

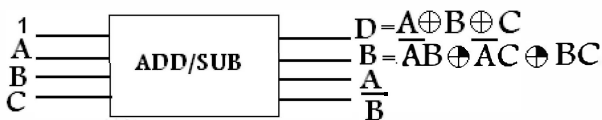


Figure 16. Reversible Full Subtractor with ADD/SUB gate

The ADD/SUB reversible gate can be used to design reversible 4-bit ripple Adder/Subtractor as shown in Figure 17 (circuit 2).

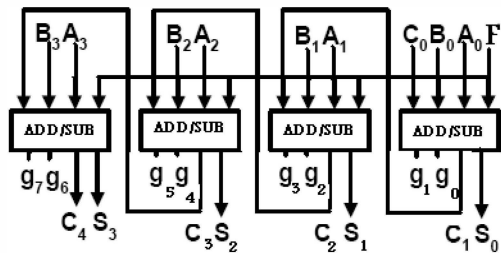


Figure 17. Reversible 4-bit Ripple Adder/Subtractor with ADD/SUB gate (circuit 2)

A comparison between the two circuits for the Reversible 4-bit Adder/Subtractor is shown in Table IV.

TABLE IV. A COMPARISON BETWEEN CIRCUIT 1 AND CIRCUIT 2

	Number of Gates	Number of Garbage
Circuit 1	8 gates	12 garbage
Circuit 2	4 gates	8 garbage

But the first design has the property that it can add/subtract both signed and unsigned numbers.

## VI. CONCLUSIONS

In this paper, we proposed two novel designs for reversible Full Adder/Subtractor. One of them can be used for signed/unsigned numbers. The other design requires only one of our proposed reversible ADD/SUB gate which produces two garbage outputs. We applied these novel reversible circuits to design a 4-bit reversible Adder/Subtractor. The proposed reversible 4-bit Adder/Subtractor circuits and the novel Reversible Full Adder/Subtractor gate (ADD/SUB gate) can be used for designing large reversible systems, which is the necessary requirement of quantum computers.

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